

WHAT IS CLAIMED IS:

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5 1. A semiconductor device comprising:  
a semiconductor layer;  
a first insulating film formed on said  
semiconductor layer;  
a first electrode layer formed on said first  
insulating layer;  
an element isolating region comprising an element  
isolating insulating film formed to extend through said  
10 first electrode layer and said first insulating film to  
reach an inner region of said semiconductor layer, said  
element isolating region isolating an element region  
and being self-aligned with said first electrode layer;  
a second insulating film formed on said first  
15 electrode layer and said element isolating region, an  
open portion exposing a surface of said first electrode  
layer being formed in said second insulating film; and  
a second electrode layer formed on said second  
insulating film and said exposed surface of said first  
20 electrode layer, said second electrode layer being  
electrically connected to said first electrode layer  
via said open portion.

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25 2. A semiconductor device comprising:  
a semiconductor layer;  
a first insulating film formed on said  
semiconductor layer;  
a first electrode layer formed on said first

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which is a semiconductor device in a memory cell array region, comprising:

said semiconductor layer;

5 said first insulating film formed on said semiconductor layer;

said first electrode layer formed on said first insulating layer;

10 said element isolating region comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer;

15 said second insulating film formed on said first electrode layer and said element isolating region; and said second electrode layer formed on said second insulating film;

20 wherein a surface of said element isolating region of said memory cell array region is arranged below a surface of said first electrode layer.

6. The semiconductor device according to claim 2, which is a semiconductor device in a memory cell array region, comprising:

25 said semiconductor layer;

said first insulating film formed on said semiconductor layer;

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memory cell array region.

9. The semiconductor device according to claim 1, wherein said first and second electrode layers comprise a gate electrode in a peripheral circuit region formed around a memory cell array region.

10. The semiconductor device according to claim 1, wherein said first and second electrode layers comprise a gate electrode in a peripheral circuit region formed around a memory cell array region, and said second insulating film of said peripheral circuit region being removed completely.

11. The semiconductor device according to claim 1, further comprising a connecting member arranged above said element isolating region and electrically connected to said second electrode layer.

12. The semiconductor device according to claim 2, further comprising a connecting member arranged above said element isolating region and electrically connected to said third electrode layer.

13. The semiconductor device according to claim 1, further comprising a connection member arranged above said element region in which said second insulating film is present and electrically connected to said second electrode layer.

14. The semiconductor device according to claim 1, further comprising a wiring electrically connected to said second electrode layer via a connecting member,



24. The semiconductor device according to claim 1, which is a semiconductor device comprising a plurality of selective transistors formed said first and second electrode layers in a NAND type flash memory, and a peripheral circuit transistor formed said first and second electrode layers,

5 said second insulating film of said plural selective transistors includes said open portion, and said second insulating film of said peripheral circuit transistor includes a plurality of said open portions, and a first distance between the adjacent open portions of said plural selective transistors is equal to a second distance between the adjacent open portions within a gate electrode of said peripheral circuit transistor.

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10 25. The semiconductor device according to claim 2, which is a semiconductor device comprising a plurality of selective transistors formed said first, second and third electrode layers in a NAND type flash memory, and a peripheral circuit transistor formed said first, 15 second and third electrode layers,

20 said second insulating film of said plural selective transistors includes said open portion, and said second insulating film of said peripheral circuit transistor includes a plurality of said open portions, and a first distance between the adjacent open portions of said plural selective transistors is equal to a second distance between the adjacent open portions within a gate electrode of said peripheral circuit transistor.

25 26. The semiconductor device according to claim 24, wherein said second distance is defined on a basis of said first distance.

27. The semiconductor device according to claim 25, wherein said second distance is defined on a basis of said first distance.

28. The semiconductor device according to claim 1, which is a semiconductor device in which a gate electrode is formed of said first and second electrode layers, and said open portion is formed in said gate electrode, wherein said open portion extends from above said element region onto said element isolating region in a direction of a channel width of said gate electrode.

29. The semiconductor device according to claim 2, which is a semiconductor device in which a gate electrode is formed of said first, second and third electrode layers, and said open portion is formed in said gate electrode, wherein said open portion extends from above said element region onto said element isolating region in a direction of a channel width of said gate electrode.

30. The semiconductor device according to claim 1, wherein a thickness of said second electrode layer when deposited is at least half a width of said open portion.

31. The semiconductor device according to claim 2, wherein a thickness of said third electrode layer when deposited is at least half a width of said open portion.

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5 32. The semiconductor device according to claim 1,  
wherein an electric resistance of said second electrode  
layer is lower than that of said first electrode layer,  
and said second electrode layer comprises of a metal  
layer including a high melting point or a lamination  
layer film comprising a metal silicide layer including  
a high melting point and a polysilicon layer.

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33. The semiconductor device according to claim 2,  
wherein an electric resistance of said second and third  
electrode layers is each lower than that of said first  
electrode layer, and said second and third electrode  
layers comprise of a metal layer including a high  
melting point or a lamination layer film comprising a  
metal silicide layer including a high melting point and  
a polysilicon layer.

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34. The semiconductor device according to claim 1,  
wherein said second insulating film comprises of a  
complex insulating film including a silicon nitride  
film.

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35. The semiconductor device according to claim 2,  
wherein said second insulating film comprises of a  
complex insulating film including a silicon nitride  
film.

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36. The semiconductor device according to claim 1,  
which is a semiconductor device in which a gate  
electrode is formed of said first and second electrode  
layers, wherein said second insulating film remains at

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~~an edge portion of said gate electrode.~~

37. The semiconductor device according to claim 2, which is a semiconductor device in which a gate electrode is formed of said first, second and third electrode layers, wherein said second insulating film remains at an edge portion of said gate electrode.

38. A semiconductor device, which is a NAND type flash memory comprising a memory cell array region provided a memory transistor including a first electrode layer performing a function of a floating gate and a second electrode layer performing a function of a control gate, and a selective gate region provided a selective transistor formed adjacent to said memory cell array region, and a peripheral circuit region arranged around said memory cell array region, said NAND type flash memory comprising:

a semiconductor layer common with said memory cell array region, said selective gate region and said peripheral circuit region;

a first insulating film formed on said semiconductor layer, said first insulating film being formed commonly with said memory cell array region, said selective gate region and said peripheral circuit region;

a first electrode layer formed on said first insulating film commonly with said memory cell array region, said selective gate region and said peripheral



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element isolating insulating film extending through  
said first electrode layer and said first insulating  
film to reach an inner region of said semiconductor  
layer, said element isolating region isolating an  
5 element region;

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isolating region and said first electrode layer;

forming an open portion within said second  
insulating film to expose a surface of the first  
10 electrode layer;

forming a second electrode layer on said second  
insulating film and said exposed surface of said first  
electrode layer; and

selectively removing said first electrode layer,  
15 said second insulating film and said second electrode  
layer to form a gate electrode.

41. A method of manufacturing a semiconductor  
device in a selective gate region provided a selective  
gate transistor formed adjacent to a memory cell array  
20 region, comprising:

forming a first insulating film on a semiconductor  
layer;

forming a first electrode layer on said first  
insulating film;

25 forming an element isolating region comprising an  
element isolating insulating film extending through  
said first electrode layer and said first insulating

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forming a third electrode layer on said second electrode layer and said exposed surface of said first electrode layer; and

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forming an element isolating region comprising an  
element isolating insulating film extending through



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58. The method of manufacturing a semiconductor device according to claim 40, wherein a surface of said

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